

## 64-BIT HIGH-VOLTAGE CMOS DRIVER

The μPD16306A is a high-voltage CMOS driver for flat display panels such as FIPs and ELs. It consists of a 64-bit bidirectional shift register, a 64-bit latch, and a high-voltage CMOS driver. The logic operates on 5 V (CMOS level input) so that it can be directly connected to a microcomputer. The drivers can output a voltage as high as 80 V at 25 mA<sub>MAX</sub>. Because both the logic and drivers are created by CMOS process, they dissipate only a tiny amount of power.

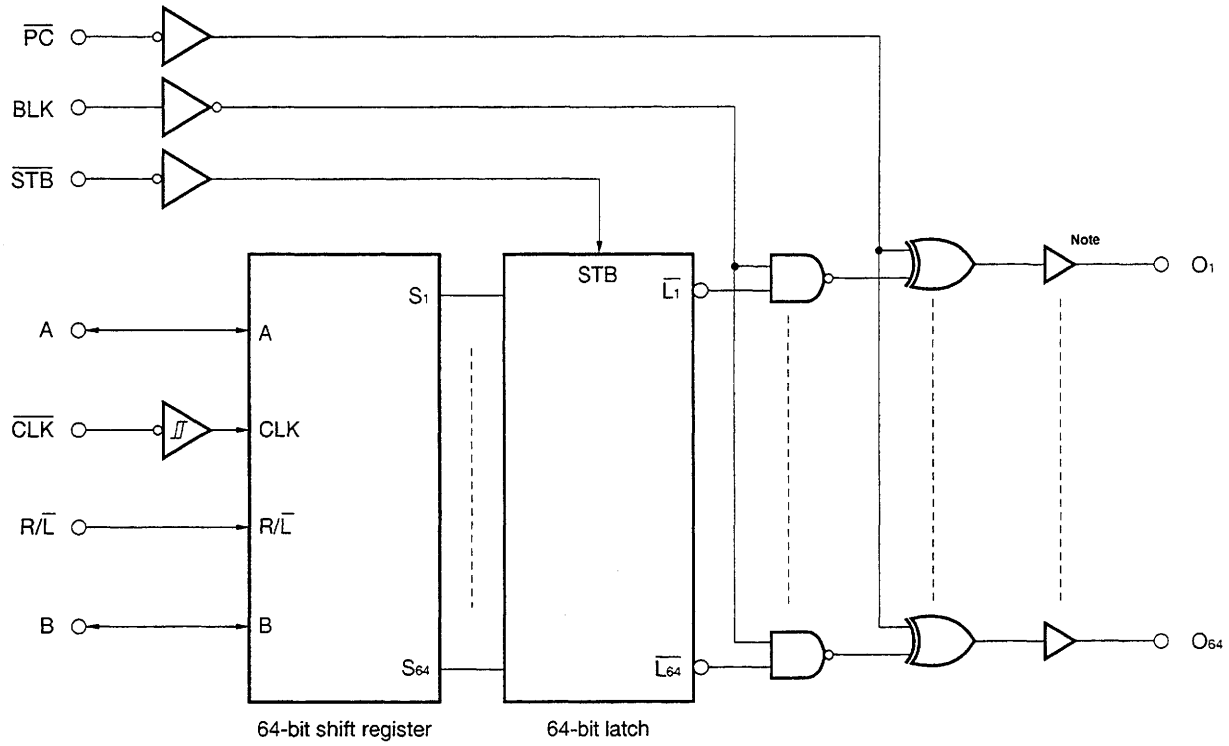
### FEATURES

- 64-bit bidirectional shift driver
- Data control through transfer lock (external) and latch
- High-speed data transfer ( $f_{\text{max.}} = 16 \text{ MHz}_{\text{MIN.}}$ , in cascade connection)
- Wide operating temperature range ( $T_A = -40$  to  $85 \text{ }^\circ\text{C}$ )
- High-voltage output (80 V, 25 mA<sub>MAX</sub>.)
- High-voltage CMOS process
- Polarities of all drivers can be reversed by using  $\overline{\text{PC}}$  pin.

### ORDERING INFORMATION

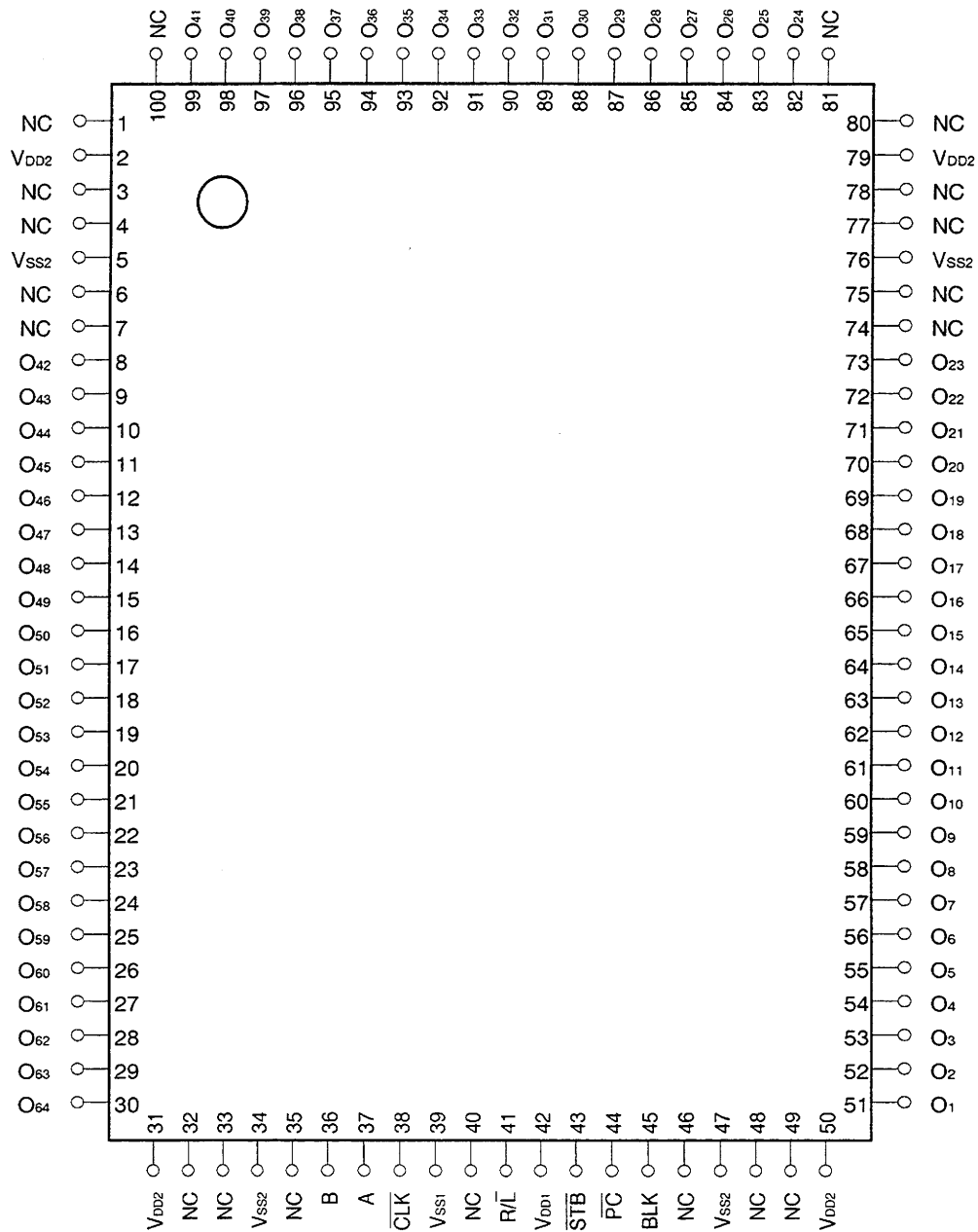
Part Number	Package
μPD16306AGF-3BA	100-pin plastic QFP (Iron lead frame: PD = 1.0 W)
μPD16306AGF-3RA	100-pin plastic QFP (Copper lead frame: PD = 1.3 W)

BLOCK DIAGRAM



**Note** High-voltage CMOS drivers (80 V ±25 mA<sub>MAX.</sub>)

PIN CONFIGURATION (Top View)



- Cautions**
1. Be sure to leave pin 40 open because it is connected to the lead frame.
  2. Be sure to use all the V<sub>DD1</sub>, V<sub>DD2</sub>, V<sub>SS1</sub>, and V<sub>SS2</sub> pins. Keep the V<sub>SS1</sub> and V<sub>SS2</sub> pins at the same voltage level.
  3. Supply power to V<sub>DD1</sub>, logic inputs, and V<sub>DD2</sub> in this order to protect the device from destruction due to latch up. Turn off power in the reverse order. Observe these power sequences even during a transition period.

**PIN FUNCTIONS**

Pin Symbol	Pin Name	Pin Number	Remark
$\overline{PC}$	Polarity reverse input	44	$\overline{PC} = L$ : Reverses polarities of all outputs
BLK	Blank input	45	BLK = H: All outputs = H or L
$\overline{STB}$	Latch strobe input	43	Through at L, holds data at H
A	RIGHT data I/O	37	$R/\overline{L} = H$ : A input, B output
B	LEFT data I/O	36	$R/\overline{L} = L$ : B input, A output
$\overline{CLK}$	Clock input	38	Executes shift at falling edge
$R/\overline{L}$	Shift direction control input	41	Right shift mode at H A → O <sub>1</sub> ... O <sub>64</sub> → B Left shift mode at L B → O <sub>64</sub> ... O <sub>1</sub> → A
O <sub>1</sub> to O <sub>64</sub>	High-voltage output	51 to 73, 82 to 99, 8 to 30	80 V 25 mA <sub>MAX.</sub>
V <sub>DD1</sub>	Logic power supply	42	5 V ± 10 %
V <sub>DD2</sub>	Driver power supply	2, 31, 50, 79	10 to 70 V
V <sub>SS1</sub>	Logic ground	39	Connected to GND of system
V <sub>SS2</sub>	Power ground	5, 34, 47, 76	Connected to GND of system
NC	Vacant pin	1, 3, 4, 6, 7, 32, 33, 35, 40, 46, 48, 49, 74, 75, 77, 78, 80, 81, 100	No connection. Be sure to leave pin 40 open.

**TRUTH TABLE 1 (SHIFT REGISTER)**

Input		I/O		Shift Register
$R/\overline{L}$	$\overline{CLK}$	A	B	
H	↓	Input	Output <b>Note 1</b>	Right shift
H	H or L		Output	Hold
L	↓	Output <b>Note 2</b>	Input	Left shift
L	H or L	Output		Hold

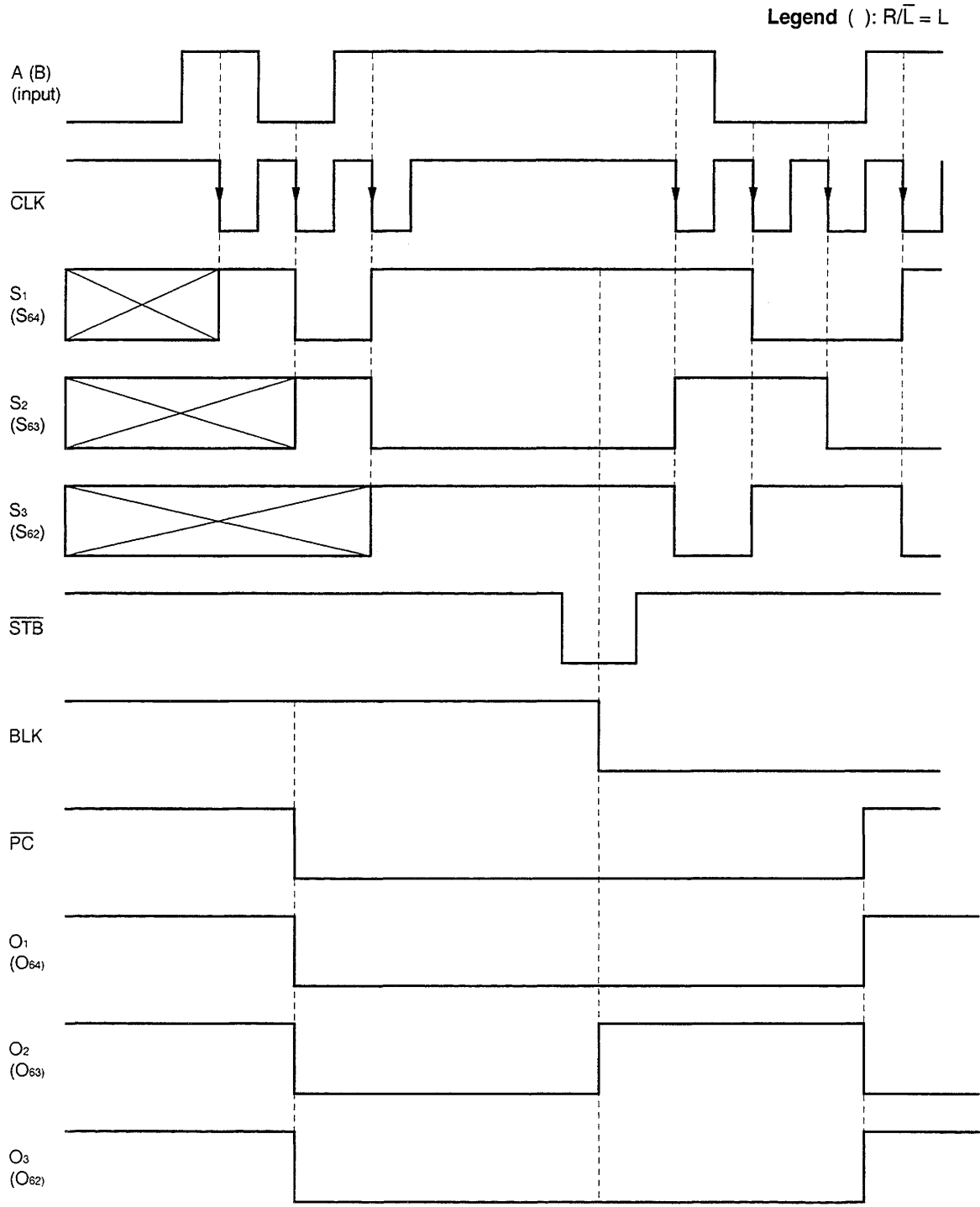
- Notes**
1. S<sub>63</sub> is shifted to the position of S<sub>64</sub> and output from B at the falling edge of the clock.
  2. S<sub>2</sub> is shifted to the position of S<sub>1</sub> and output from A at the falling edge of the clock.

**TRUTH TABLE 2 (LATCH AND DRIVER)**

Input				Driver Output Stage
A (B)	$\overline{STB}$	BLK	$\overline{PC}$	
X	X	H	H	H (all drivers: H)
X	X	H	L	L (all drivers: L)
H	L	L	H	H
H	L	L	L	L
L	L	L	H	L
L	L	L	L	H
X	H	L	H	Outputs data immediately before $\overline{STB}$ goes to H
X	H	L	L	Reverses and outputs data immediately before $\overline{STB}$ goes to H

**Remark** X = H or L, H = high level, L = low level

TIMING CHART



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Rating	Unit
Logic supply voltage	V <sub>DD1</sub>	-0.5 to +7.0	V
Logic input voltage	V <sub>I</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Logic output voltage	V <sub>O1</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver supply voltage	V <sub>DD2</sub>	-0.5 to 80	V
Driver output voltage	V <sub>O2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Driver output current	I <sub>O2</sub>	± 25	mA
Permissible package dissipation	P <sub>D</sub>	1000	mW
Operating temperature range	T <sub>A</sub>	-40 to +85	°C
Storage temperature range	T <sub>stg.</sub>	-65 to +150	°C

**RECOMMENDED OPERATING RANGE (T<sub>A</sub> = -40 to 85 °C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V <sub>DD1</sub>	4.5	5.0	5.5	V
High-level input voltage	V <sub>IH</sub>	0.7 · V <sub>DD1</sub>		V <sub>DD1</sub>	V
Low-level input voltage	V <sub>IL</sub>	0		0.2 · V <sub>DD1</sub>	V
Driver supply voltage	V <sub>DD2</sub>	10		70	V
Driver output current	I <sub>OL2</sub>			+20	mA
	I <sub>OH2</sub>			-20	mA

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, V<sub>DD1</sub> = 5.0 V, V<sub>DD2</sub> = 70 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level output voltage	V <sub>OH1</sub>	Logic I <sub>OH1</sub> = -1.0 mA	0.9 · V <sub>DD1</sub>			V
Low-level output voltage	V <sub>OL1</sub>	Logic I <sub>OL1</sub> = 1.0 mA			0.1 · V <sub>DD1</sub>	V
High-level output voltage	V <sub>OH21</sub>	O <sub>1</sub> to O <sub>64</sub> , I <sub>OH2</sub> = -0.5 mA	69			V
	V <sub>OH22</sub>	O <sub>1</sub> to O <sub>64</sub> , I <sub>OH2</sub> = -5.0 mA	65			V
Low-level output voltage	V <sub>OL21</sub>	O <sub>1</sub> to O <sub>64</sub> , I <sub>OL2</sub> = 2.5 mA			1.0	V
	V <sub>OL22</sub>	O <sub>1</sub> to O <sub>64</sub> , I <sub>OL2</sub> = 20 mA			10	V
High-level input current	I <sub>IH</sub>	V <sub>I</sub> = V <sub>DD1</sub>			1.0	μA
Low-level input current	I <sub>IL</sub>	V <sub>I</sub> = 0 V			-1.0	μA
High-level input voltage	V <sub>IH</sub>		0.7 · V <sub>DD1</sub>			V
Low-level input voltage	V <sub>IL</sub>				0.2 · V <sub>DD1</sub>	V
Static current dissipation	I <sub>DD1</sub>	Logic, T <sub>A</sub> = 25 °C			10	μA
	I <sub>DD1</sub>	Logic, T <sub>A</sub> = -40 to +85 °C			100	μA
	I <sub>DD2</sub>	Driver, T <sub>A</sub> = 25 °C			100	μA
	I <sub>DD2</sub>	Driver, T <sub>A</sub> = -40 to +85 °C			1000	μA

**SWITCHING CHARACTERISTICS**

( $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD1} = 5.0\text{ V}$ ,  $V_{DD2} = 70\text{ V}$ ,  $V_{SS1} = V_{SS2} = 0\text{ V}$ , logic  $C_L = 15\text{ pF}$ , driver  $C_L = 50\text{ pF}$ )

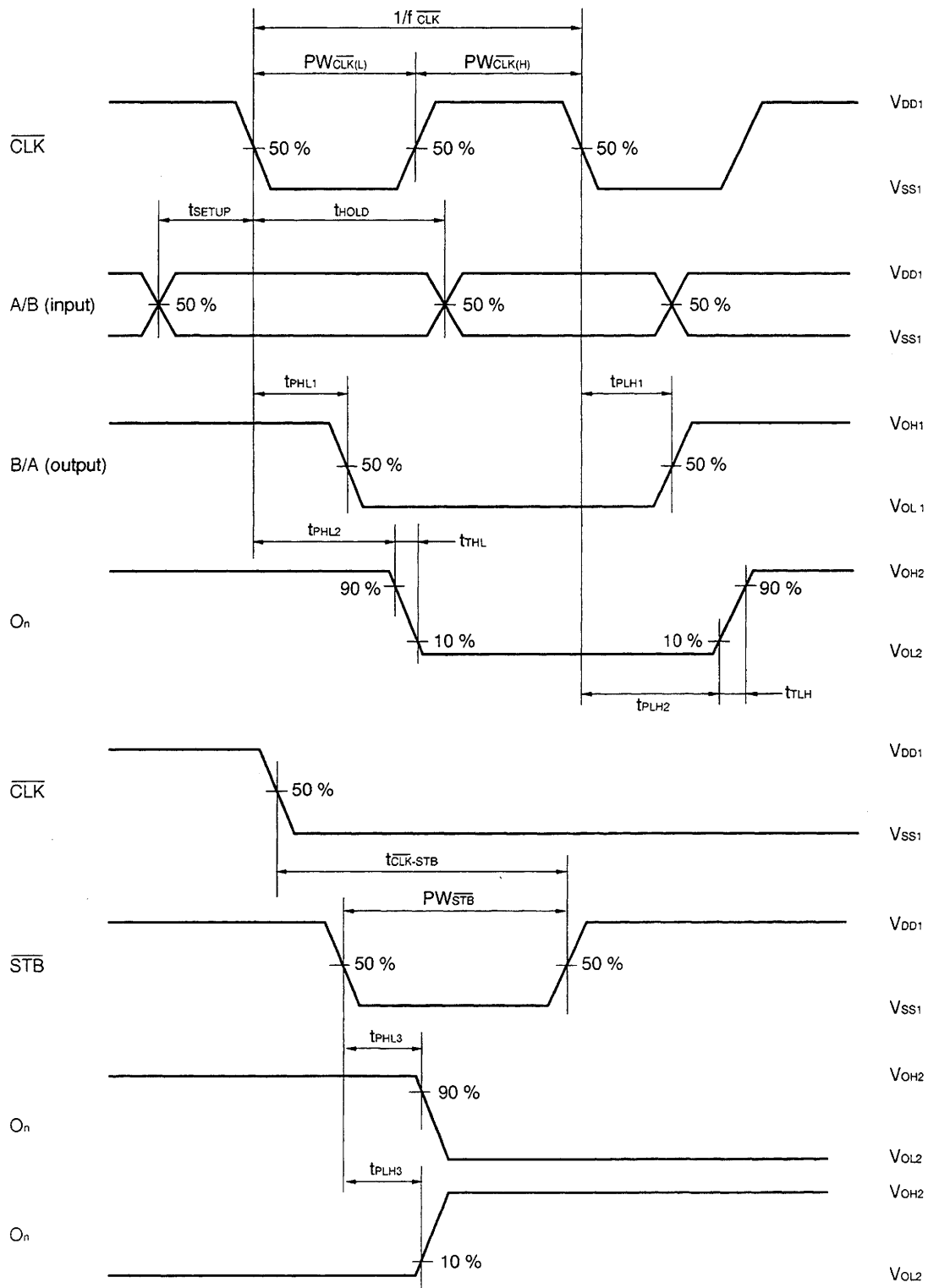
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Propagation delay time	$t_{PHL1}$	$\overline{CLK} \rightarrow A/B$			50	ns
	$t_{PLH1}$				50	ns
	$t_{PHL2}$	$\overline{CLK} \rightarrow O_1 \text{ to } O_{64}$			300	ns
	$t_{PLH2}$				300	ns
	$t_{PHL3}$	$\overline{STB} \rightarrow O_1 \text{ to } O_{64}$			300	ns
	$t_{PLH3}$				300	ns
	$t_{PHL4}$	$BLK \rightarrow O_1 \text{ to } O_{64}$			300	ns
	$t_{PLH4}$				300	ns
	$t_{PHL5}$	$\overline{PC} \rightarrow O_1 \text{ to } O_{64}$			300	ns
	$t_{PLH5}$				300	ns
Rise time	$t_{TLH}$	$O_1 \text{ to } O_{64}$			200	ns
Fall time	$t_{THL}$	$O_1 \text{ to } O_{64}$			200	ns
Maximum clock frequency	$f_{max.}$	Duty = 50%, data loading	25			MHz
		In cascade connection	16			MHz
Input capacitance	$C_i$				20	pF

**TIMING REQUIREMENTS**

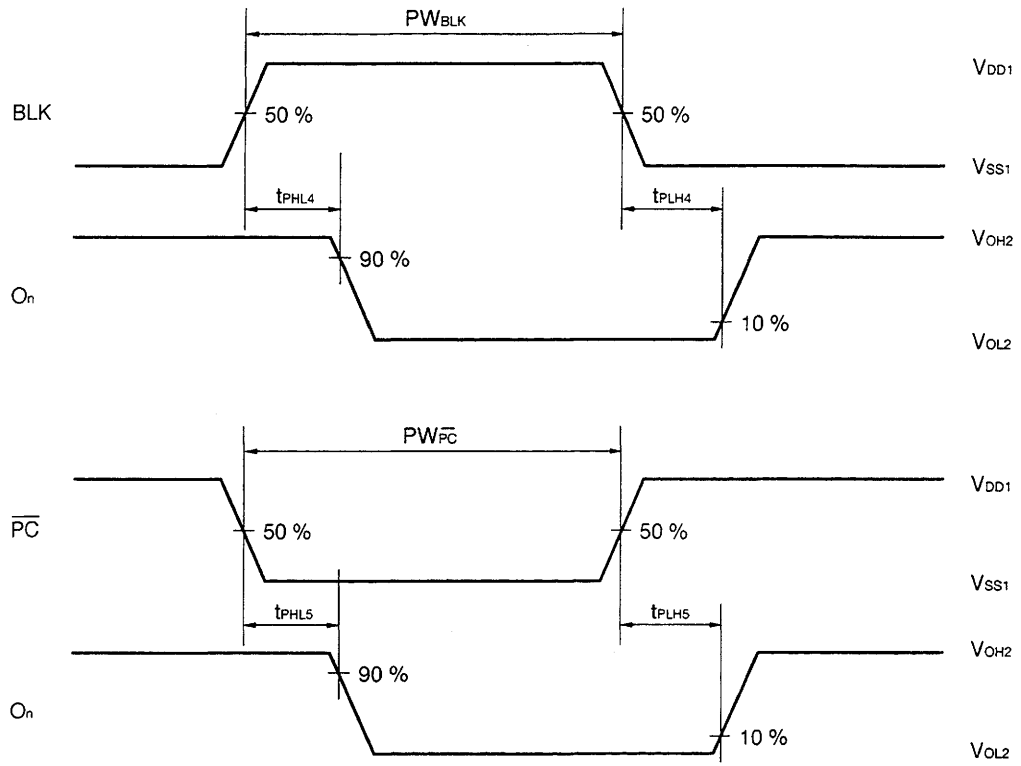
( $T_A = -40 \text{ to } 85\text{ }^\circ\text{C}$ ,  $V_{DD1} = 4.5 \text{ to } 5.5\text{ V}$ ,  $V_{DD2} = 10 \text{ to } 70\text{ V}$ ,  $V_{SS1} = V_{SS2} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock pulse width	$PW_{\overline{CLK}}$		20			ns
Strobe pulse width	$PW_{\overline{STB}}$		20			ns
Blank pulse width	$PW_{BLK}$		560			ns
$\overline{PC}$ pulse width	$PW_{\overline{PC}}$		560			ns
Data setup time	$t_{SETUP}$		10			ns
Data hold time	$t_{HOLD}$		10			ns
Clock-strobe time	$t_{\overline{CLK-STB}}$	$\overline{CLK} \downarrow \rightarrow \overline{STB} \uparrow$	50			ns

SWITCHING CHARACTERISTIC WAVEFORMS



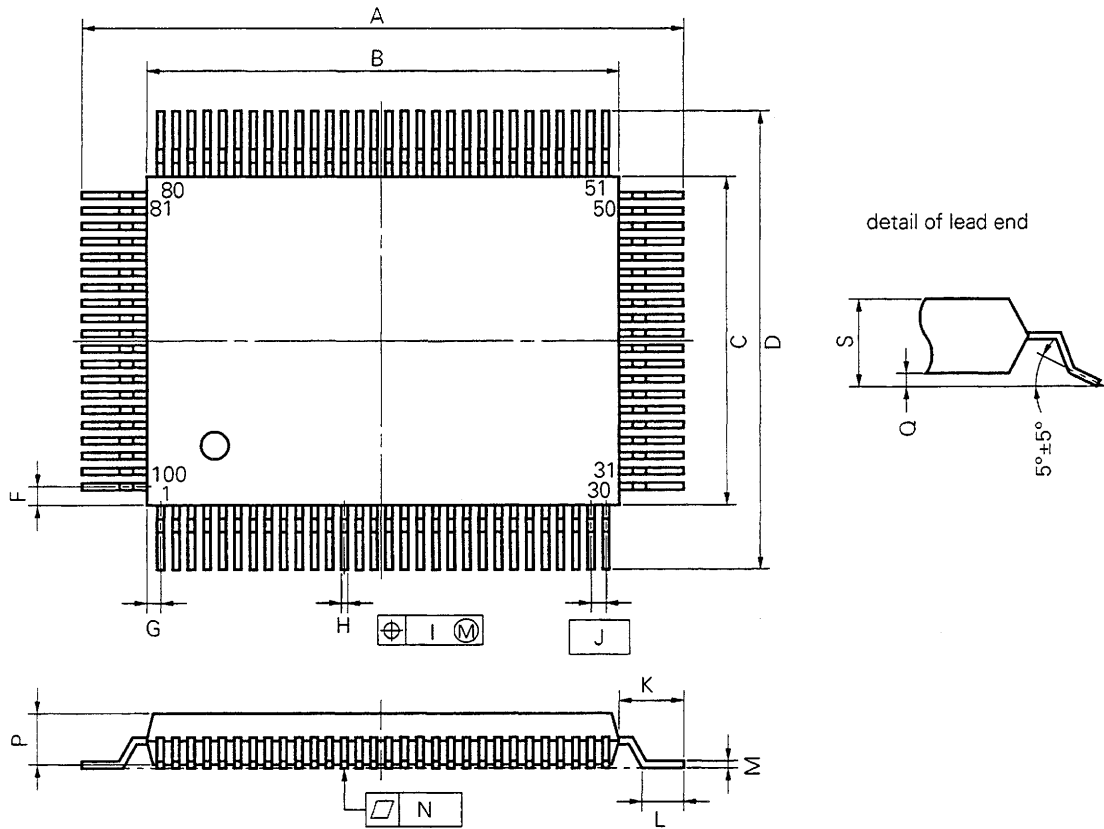




PACKAGE DRAWING

μPD16306AGF-3BA (Iron lead frame)

100 PIN PLASTIC QFP (14x20)



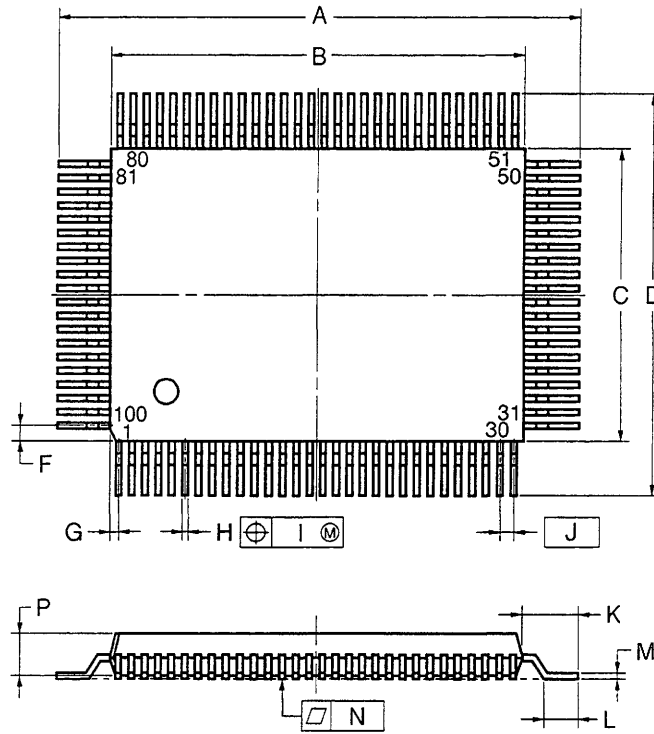
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

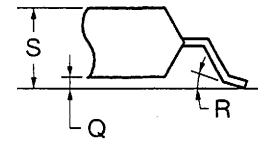
P100GF-65-3BA-2

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 <sup>+0.009</sup> / <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> / <sub>-0.008</sub>
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012 <sup>+0.004</sup> / <sub>-0.005</sub>
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	0.071 <sup>+0.008</sup> / <sub>-0.009</sub>
L	0.8±0.2	0.031 <sup>+0.009</sup> / <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> / <sub>-0.05</sub>	0.006 <sup>+0.004</sup> / <sub>-0.003</sub>
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

**PACKAGE DRAWING**  
**μPD16306AGF-3RA (Copper lead frame)**  
**100 PIN PLASTIC QFP (14×20)**



detail of lead end



**NOTE**

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	0.913 <sup>+0.009</sup> <sub>-0.008</sub>
B	20.0±0.2	0.787 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.2±0.2	0.677±0.008
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S100GF-65-3BA-3

**RECOMMENDED SOLDERING CONDITIONS**

Please perform the soldered mounting of this product under the following recommended conditions.

For soldering methods and conditions other than those recommended here, please contact your NEC sales representative.

**Surface Mount Type**

For details on recommended soldering conditions, please refer to the “**Semiconductor Device Mounting Technology Manual**” (C10535E).

**μPD16306AGF-3BA**

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared Reflow	Package peak temperature: 235 °C, time: up to 30 sec. (no less than 210 °C), count: once, restricted number of days: none <b>Note</b>	IR-35-00-1
VPS	Package peak temperature: 215 °C, time: up to 40 sec. (no less than 200 °C), count: once, restricted number of days: none <b>Note</b>	VP15-00-1
Pin Part Heating	Pin part temperature: no more than 300 °C, time: up to 10 sec., restricted number of days: none <b>Note</b>	

**Note** This refers to the restricted number of days for storage after decapsulating the dry pack. The storage conditions are no more than 25 °C and 65 % RH.

**Caution** Please avoid mixing use of soldering methods (except for pin part heating methods).

**References**

- NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)
- Quality Grades of NEC Semiconductor Devices (IEI-1209)
- Semiconductor Device Mounting Technology Manual (C10535E)

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